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Implementation of a strategy to improve the efficiency of battery chargers with double conversion topology, high power factor, and low THDi

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ABSTRACT

This paper presents a comparison between different Power Factor Correction topologies (PFC), highlighting the main advantages and disadvantages of the implementation requirements for a battery charger. Subsequently, the cascade connection of boost and buck converters is selected, for which a detailed loss analysis is performed, whose results are used to develop an operating strategy that allows the controller to act on a range of combinations of duty cycles to maximize the efficiency of the converters, maintaining adequate levels of voltage and current regulation, efficient regulation of battery recharge, high power factor, and low THDi. Finally, this converter is implemented with the mentioned operating strategy to perform constant power battery recharging, and the experimental results are presented with special emphasis on efficiency, power factor, and THDi, the latter being compared with the IEC 61000-3-2 standard.

1. Introduction

Countries such as Norway, France, the United Kingdom, Japan, and China expect that by 2050, 50% of their vehicle fleet will be electric [1] which promotes the use of electronic switching elements for recharging, bringing in turn serious consequences on power quality. Among the main negative consequences on power quality are high THD levels in current, which in turn can generate distortion in voltage levels, increase losses in conductors, and trigger protection systems, among others [2].

Modular multilevel converters (MMCs) have attracted the attention of engineers and researchers. This interest lies in the inherent suitability of MMCs for large-scale renewable energy integration and their ease of interconnecting AC power with DC elements [3]. Within the CMMs, there is a subgroup called the cascaded CMMs, which consist of the cascaded connection of two or more classical converters such as the Cük presented in [4] where a special control technique is applied to deduce the size of the output capacitor, the bridgeless SEPIC [5], the flyback [6], the totem-pole bridgeless PFC (TPBPFC) [7], among others. The latter have notable advantages as shown in [8] where a comparative study of different boost converters, including the cascaded boost, is made and it is concluded that although it is not the one with the highest conversion rate, it is the most efficient among the converters covered by this study. Similarly, the use of cascaded converters works as a strategy to obtain good conversion rates using several reactive elements whose values are not as large as those that would be had in other types of converters seeking the same conversion rate, as shown in [9].

On the other hand, some converters have within their structure a high-frequency transformer, which generates galvanic isolation between input and output, but at the same time can generate interference problems and additionally, EMI losses would also take place. Despite not having galvanic isolation, dual converter topologies have the possibility of presenting a high impedance between the input and output stage through a suitable controller [9] and thus avoid the problems listed above, not to mention its greater simplicity of construction and control.

Despite the mentioned advantages of cascaded converters, there are also challenges to be addressed and one of them is

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stability, because despite having the converters operating individually properly, when connected in cascade stability problems arise in the operation, so it is necessary to take this into account in the design of the controller. The impedance method for stability of this type of topology is an attractive alternative [10], although the constant power load (CPL) concept [11] simplifies the stability analysis and controller design by considering the regulating converter as a CPL in a certain frequency range.

On the other hand, the cascade converter topology has the characteristic that for a given input and output voltage value, it is possible to have multiple combinations of duty cycles (D) (one for each converter) to fulfill the voltage transformation task. In different situations, these D are chosen based on the operating limitations of some of its elements. Alternatively, when the cascaded converters are of the same type, it is also possible to set the same D for each of the converters, thus simplifying the decision and control, as shown in [12].

Considering the efficiency and stability challenges exposed for cascaded converters, this paper shows the design, control, and experimental results of a battery charger composed of a cascaded boost and buck converter operating as a low THDi power factor corrector, which from a detailed loss analysis, develops a loss mitigation strategy that finds an adequate range of duty cycles combination of the converters that allows it to operate with high efficiency, while at the same time presents a wide stability margin. Additionally, it meets the minimum requirements of a charger such as a low ripple output current for battery recharging.

This paper is organized as follows: initially, a brief review of the topologies considered as the most suitable for PFC battery chargers is shown, and then the selection criteria that lead to the choice of the cascaded converter topology that will be implemented. Then a loss analysis is performed for the two converters chosen. In the next section, the strategy that allows for obtaining the maximum efficiency is elaborated, and then the details of the controller elaboration as well as its stability analysis and charger construction are presented. Finally, the experimental results and their respective analysis are shown.

2. Selection of conversion topologies

The input topology comprising the cascade converter is the Boost converter because it has a coil at its input, which facilitates the control of the input current, and this, in turn, makes it conducive to correcting the power factor and keeping the THDi low. As for the output converter, the Buck converter was chosen due to its simplicity and the need to be able to reduce the voltage values delivered by the boost converter, which by their nature are higher than 170 V for the Colombian grids. Additionally, the purpose of the buck converter is also to reduce the output current ripple.

Having chosen a dual boost-buck converter cascading topology illustrated in Fig. 1, it is convenient to establish which of the different boost variations would be the most appropriate for building a battery charger acting as a PFC. In this sense, the attention of the study is focused on the most representative PFC boosts, which are analyzed through the criteria: efficiency, simplicity, ease of control, protection, and implementation cost.

Framed by the above-mentioned criteria, the following comparative analysis is presented based on [13]. This analysis focuses on the data shown in Table 1, whose information presents the number of semiconductor components and their type (low or high frequency), for each of the PFCs considered and shown in Fig. 2. Recalling that efficiency is a highly relevant aspect within the considerations made. Table 1 includes the number of elements that are active in the ON and OFF states of the converter to have an estimate of the conduction and switching losses.

By purchasing the results shown in Table 1, the conventional BPFC topology stands out as one of those with the lowest number of semiconductor elements, since it has only 4 and zero high and low-frequency components, respectively. The other two topologies with only four high-frequency semiconductor components are BPFC clamped (C) with coupling inductor and BPFC clamped (C), but these have 2 and even 3 extra elements that increase not only their cost but possibly the losses inside the converter.

Thus, the conventional BPFC topology stands out among its peers due to favorable features such as the lack of a specific rectification stage, making the current flow through only two semiconductors at a time. In addition, one of these diodes serves as an anti-return element toward the grid, which is a recommendation for the construction of battery chargers [13]. Despite this, it also presents a drawback of having a higher common mode noise than the PFC rectifier, because in the boost rectifier the negative of the output is always connected to the AC source through the bridge rectifier, while for the conventional BPFC, the output is connected to the AC source only in the positive half-cycle through the switch diode S2 and in the negative cycle, the negative of the output is pulsed concerning the AC source (with high frequency) as shown in Fig. 3. This high frequency pulsing in the voltage charge and discharge parasitic capacitance between the output negative and the AC source is what increases the common mode noise.

Given the existing difficulty for the conventional BPFC topology, an alternative is to add a second inductor, as shown in Fig. 2e, which results in two boost circuits (one for each cycle) and adding two slow recovery diodes at the grid terminals to ensure a permanent connection between the output and the grid. Similarly, better thermal performance is attributed to having two inductors, since less heating is generated in the cores, which in turn implies lower losses.

On the other hand, another topology that also has only four switching elements is the totem pole represented in Fig. 2b, how-

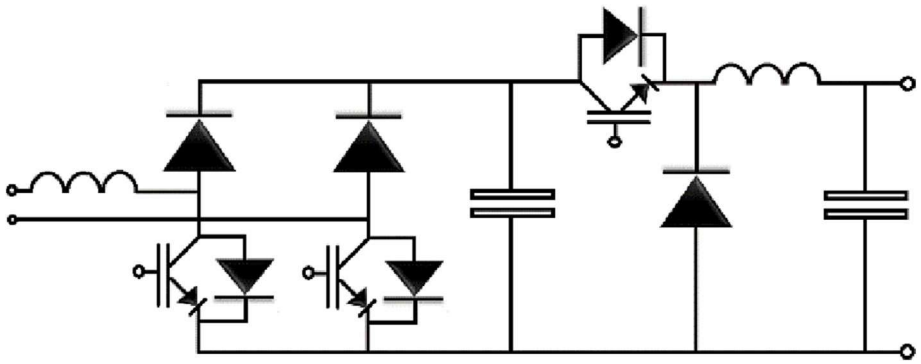

Fig. 1. Boost-buck cascade topology. Source: Authors.

Table 1
Comparative summary of boost topologies, according to the number of elements and their type [14].

ID	Topology	ON		OFF		Semiconductors LF	Semiconductors HF	Components Additional
		Diode	MOSFET	Diode	MOSFET			
a	Conventional PFC	2	1	3	0	4	2	0
b	Conventional BPFC	0	2	1	1	0	4	0
c	BPFC with additional switch	0	2	1	2	0	5	0
d	BPFC with zero active branch	2	1	1	1	0	9	0
e	BPFC clamped diode	1	1	2	0	2	4	0
f	BPFC clamped diode with common core inductor	1	1	2	0	2	4	0
g	Totem pole	1	1	1	1	2	2	0
h	BPFC clamped (C)	0	2	1	1	0	4	2
i	BPFC clamped (C) with coupling inductor	0	2	1	1	0	4	3
j	BPFC with active virtual ground	0	2	1	1	2	4	1

ever, unlike all bridgeless topologies, this one can only operate in Discontinuous conduction mode Discontinuous Conduction Mode (DCM) and Boundary Conduction Mode (BCM) due to the arrangement of the switches. The reverse diode recovery of the MOSFETs makes Continuous Conduction Mode (CCM) operation impractical, and operating in DCM makes modeling, control, and management of the THDi difficult, thus ruling out this topology for this work.

Returning, to the conventional BPFC, it must be said that the two switches are controlled by the same PWM signal, which simplifies the control task and is also less sensitive to noise because the gate drivers are referenced to the ground. Additionally, it has the coil at the converter input, which facilitates the charger input current control and is to obtain good THDi and PF values.

Thus, the conventional BPFC is chosen as the most suitable converter for the construction of the PFC charger, to which a buck converter will be cascaded. Next, the joint operation of the two converters is analyzed and it is highlighted the fact that the output of the first converter has the AC port power pulse of twice the frequency of the network (50 Hz or 60 Hz) thus generating what is known as second harmonic current (SHC). This SHC will propagate through the first converter until it reaches the load or DC source which can cause increased stress on the switching elements and on the load itself which in this case is a battery, thus compromising the life of these elements [15]. To minimize this effect the impedance of the second converter will be increased through the controller, although in this way the SHC is forced to flow through the output capacitor of the first stage converter, which in turn would force it to choose high capacitance values for this element and thus decrease the voltage ripple, however, it is not necessary in this case, because the second converter will be responsible for regulating the output voltage despite the variation of the output voltage of the first converter.

3. Analysis of losses in converters

As mentioned above, high THDi and low PF have an impact on converter efficiency, however, switching techniques and losses inherent to the characteristics of the elements have the greatest impact on this aspect. It is for this reason that in this section a detailed analysis of the losses in the converters is presented to then use this information within an efficiency and control strategy, as explained in the following section.

3.1. Losses in the boost converter

It starts with the boost stage of the loader following [16] for the derivation of the formulas presented here. The first group of losses to be analyzed are those occurring in the transistor (P_T), these being conduction (P_{Ron}) and switching (P_{sw}), which can be condensed in equation (1).

$$P_T = P_{Ron} + P_{sw} = \left(\frac{D \cdot R_{DS}}{(1-D)^2 \cdot R} + \frac{1}{2} f \cdot C_0 \cdot R\right) P_0 \tag{1}$$

Where R_{DS}: drain-source resistor, C_0: equivalent transistor output capacitance, P_0 : output power and *R:* load. This last parameter must be readjusted considering that the load will be the buck converter and that we will work on a constant power scheme.

On the other hand, the losses occurring in the diodes (P_D) correspond to the internal conduction resistance, which turns out to be dynamic (P_{fr}), and to the forward voltage drop (V_f) of the diode (P_{fv}). These losses are represented mathematically by equation (2).

$$P_D = P_{fv} + P_{fr} = \left(\frac{V_f}{V_o} + \frac{R_f}{(1-D) \cdot R}\right) P_0 \tag{2}$$

The passive elements of the converter also present losses, which in the case of the capacitor (P_c) are due to the Equivalent Series Resistance ESR or equivalent series resistance (R_c) whose value is frequency dependent. The losses associated with this element are expressed through equation (3).

$$P_c = \frac{D \cdot R_c \cdot P_o}{(1-D)^2 \cdot R} \tag{3}$$

While in the case of the inductor, its losses (P_L) are given by equation (4), where R_L represents the winding resistance. It should be clarified that losses due to the core will be disregarded for this analysis.

$$P_L = \frac{R_L . P_o}{(1-D) \cdot R} \tag{4}$$

3.2. Losses in the buck converter

For the buck converter, [17] is used as a procedural guide in its asynchronous buck converter section, from which the results shown here are obtained. Starting his time with the conduction losses in the diode (P_{ON-D}), which takes place when the transistor is open since this is when the diode conducts, so the higher the converter voltage drop rate, the more the diode will operate and these losses will predominate, while the recovery losses (P_{D-r}) are directly proportional to the switching frequency, as indicated by equation (5).

$$P_{ON-D} + P_{D-r} = I_{out} . V_F \left(1 - \frac{V_{out}}{V_{in}}\right) + \frac{V_{IN} \cdot I_{RR} \cdot t_{RR} \cdot f}{2} \tag{5}$$

When analyzing the switching element, which for this case is a MOSFET, this starts with the losses due to the output capacitance in the MOSFET (P_{COSS}), which is generated when the capacitance of the MOSFET is loaded with C_{DS-H} being the drain-source capacitance and C_{GD-H} being the gate-drain capacitance.

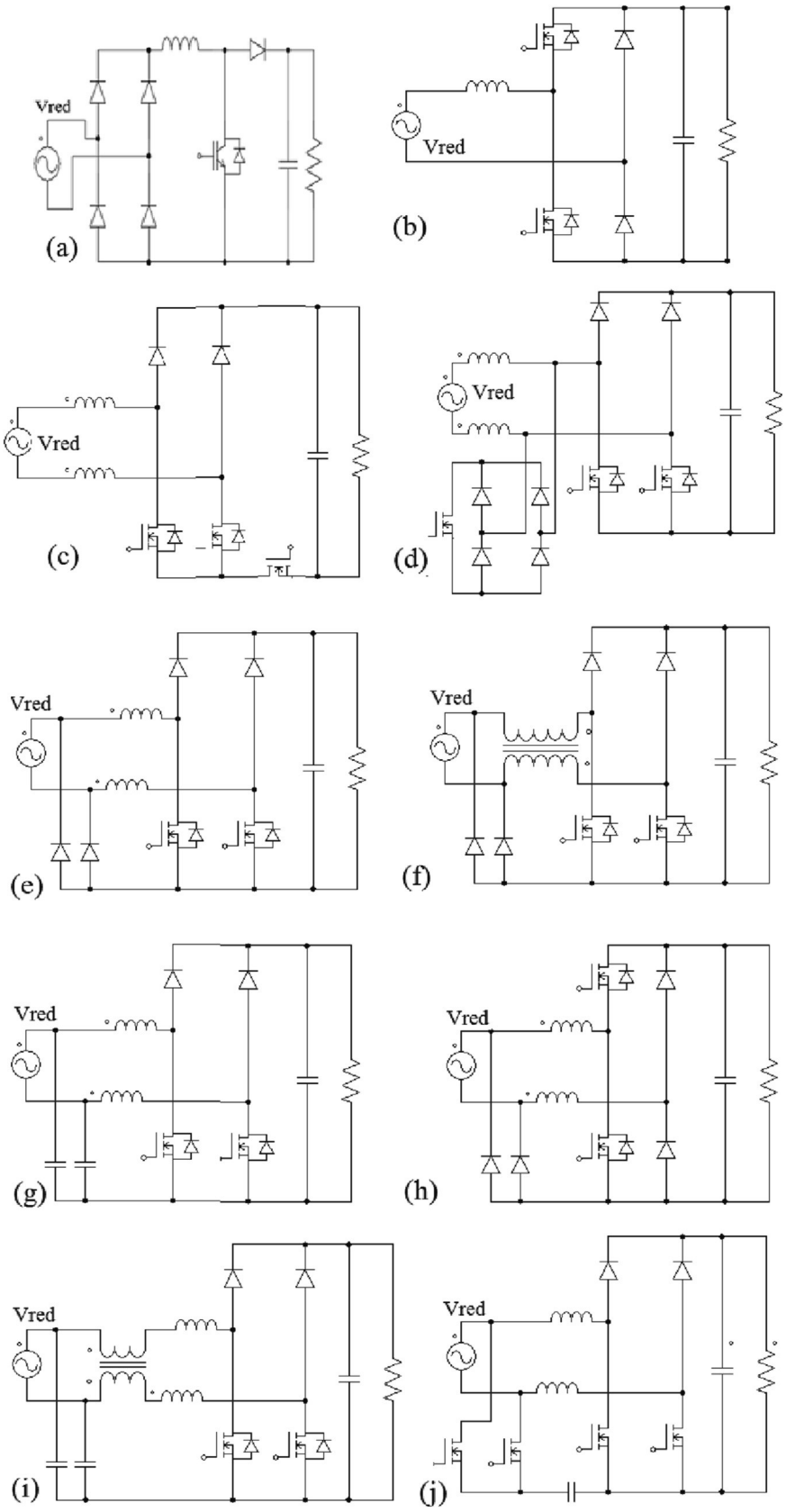

Fig. 2. Diagrams of the main boost type PFC topologies. Source: Authors.

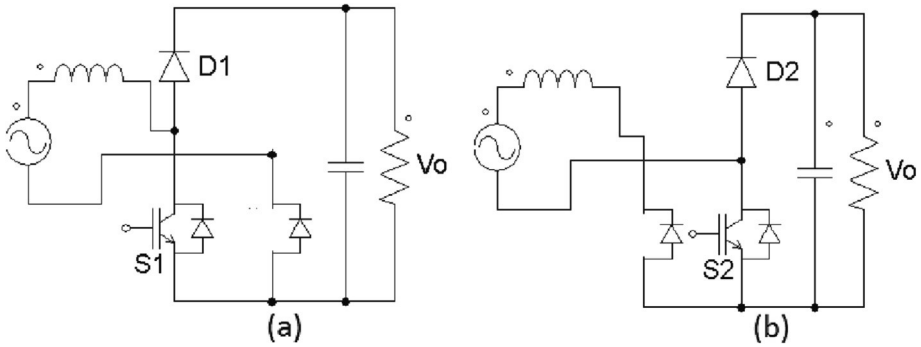

Fig. 3. Operation of the PFC without a bridge. Source: Authors.

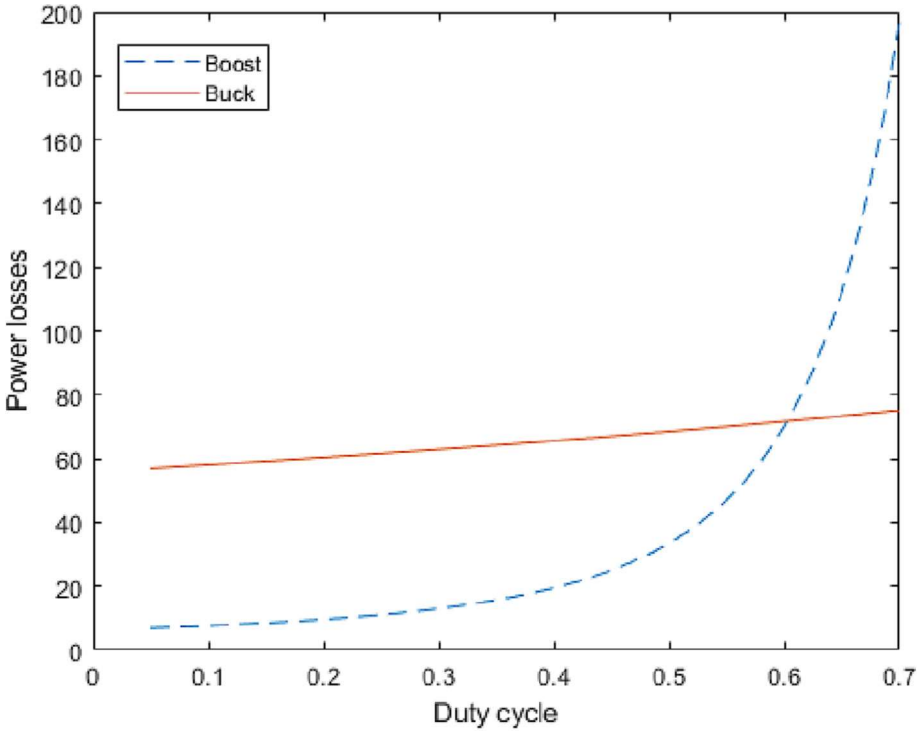

Fig. 4. Buck and boost losses for different values of duty cycle. Source: Authors.

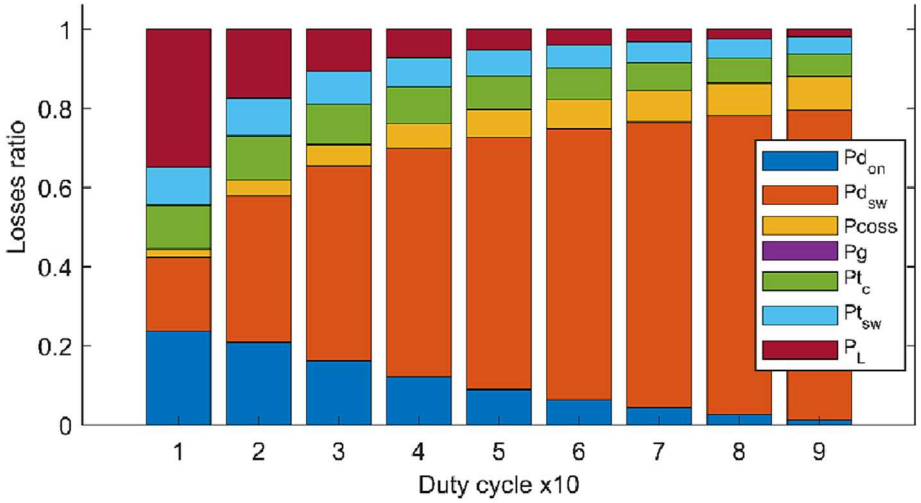

Fig. 5. Normalized losses for the buck converter for different values of the duty cycle for an input of 300 V and a load of 36.36 Ω. Source: Authors.